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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,896	10/31/2003	Frederick A. Perner	200311702-1	3008

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EXAMINER	
BRITT, CYNTHIA H	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 06/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/698,896	PERNER ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 31 October 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10/31/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-17 are presented for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, the phrase "the read circuit including a digital counter having an output that indicates a single bit" is not clear to the examiner.

As per claim 2, the phrase "an output of the digital sense amplifier connected to an input of the digital counter during the normal mode of operation." seems to be missing a verb.

As per claim 5, in line 3 the word store is unclear and possibly should read "stored".

Claims 2-8 are dependent on claim 1 and inherit the 35 U.S.C. 112, second paragraph issues of the independent claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baker U.S. Patent No. 7,009,901.

As per claims 1, 9, 10, 15, and 16, Baker substantially teaches the claimed non-volatile memory, system and method where an existing type of read circuit 200 for sensing the resistance values and thereby reading data from the memory cells 102 in the MRAM array 100 of FIG. 1. In FIG. 2, the same selected memory cell 102 discussed

with reference to FIG. 1B is assumed to be selected and thus the equivalent circuit of FIG. 1B is shown as providing sense voltage SV as an input to the read circuit 200. A sense amplifier 202 receives the sense voltage SV from the selected bit line BL3 and generates a pulse clocking signal PCLK which has a frequency of pulses that is a function of the value of the sense voltage SV. A counter 204 receives the PCLK signal and generates a sense count SCNT responsive to each pulse of the PCLK signal. The counter 204 applies the SCNT count to a latch 206 which latches the SCNT count responsive to a latch count signal LC from a reference counter 208. The reference counter 208 is clocked by an applied clock signal CLK and activates the LC signal when an internal count equals a predetermined value, which occurs after a predetermined number of cycles of the CLK signal and thus after a predetermined time T. In this way, the reference counter 208 activates the LC signal to latch the SCNT every T seconds. The counter 204 resets the SCNT count responsive to the LC signal going active. A comparator 210 compares the latched SCNT from the latch 206 to a reference count RCNT and generates a data signal D responsive to this comparison. The RCNT count has a value corresponding to a threshold value for the resistance of the selected memory cell 102. When the SCNT is greater than the RCNT count, the comparator 210 drives the data signal D high, and when the SCNT count is less than the RCNT count the comparator drives the data signal low. (Figure 2, column 3 lines 25-56) Not disclosed by Baker is that this is done in a test mode however it would have been obvious to one of ordinary skill in the art at the time this invention was made to

differentiate the test mode from the normal mode because it would be necessary for normal operation of the circuit.

As per claim 2, Baker teaches the read circuit further includes a digital sense amplifier for performing the multi-sample read operations, an output of the digital sense amplifier connected to an input of the digital counter during the normal mode of operation. (Column 3 lines 50-56)

As per claim 3, Baker teaches the performing a multi-sample read operation includes using the digital sense amplifier to take a first sample and cause a state of the digital counter to represent the result of the first sample; using the digital sense amplifier to establish a reference count, and making a comparison of the digital counter state to the reference count. (Column 3 lines 30-40)

As per claim 4, Baker teaches the read circuit further includes a sample/hold for shifting the digital counter state between the sample/hold and the digital counter, and for inverting the sign of its state. (Figure 2 element 206)

5. The device of claim 2, wherein the digital sense amplifier includes an integrator for integrating a charge at a rate that is dependent upon a logic value store in a selected memory device; and wherein the state of the digital counter is changed at a rate that is proportional to the integration time.

6. The device of claim 1, wherein the single bit is a sign-bit of the digital count.

As per claim 7, it is well known it the art for nonvolatile memory to include a resistive cross point array of memory cells as the prior art is replete with such reference this would merely be a design choice of the inventor.

As per claim 8, The device of claim 1, it is well known it the art for nonvolatile memory to include an MRAM array of memory cells as the prior art is replete with such reference this would merely be a design choice of the inventor.

As per claims 11-14 Baker teaches, the counter 204 continues incrementing the SCNT count in response to pulses of the PCLK signal. Because the PCLK signal has a frequency determined by the value of the sense voltage SV which, in turn, is determined by the resistance of the selected memory cell 102, the SCNT count is incremented at a rate determined by the resistance of the selected memory cell. At the same time, the reference counter 208 increments the internal count responsive to the CLK signal. The counters 204, 208 continue incrementing their respective counts in response to the PCLK and CLK signals until the internal count generated by the reference counter equals a predetermined value. The reference counter 208 increments the internal count once each cycle of the CLK signal, and thus the internal count equals a predetermined value after a predetermined number of cycles of the CLK signal, which occurs after a predetermined time T. Once the internal count of the reference counter 208 equals the predetermined value, the counter activates the LC signal causing the latch 206 to store the SCNT count at this point. The rate at which the SCNT count is incremented and thus the value of the latched SCNT count depends on the frequency of the PCLK signal which, in turn, depends on the value of the sense voltage SV. In this way, the counter

204 increments the SCNT count responsive to the PCLK signal for the time T, and at this point the value of the SCNT count is stored by the latch 206 and provided to the comparator 210. The comparator 210 compares the latched SCNT count to the reference count RCNT and drives the signal D either high or low depending on this comparison. When the latched SCNT count has a value that is less than the RCNT count, the sense voltage SV and thus the resistance RSC of the selected memory cell 102 corresponds to a first logic state and the comparator 210 drives the data signal D low, indicating the selected memory cell stores the first logic state. In contrast, when the latched SCNT count is greater than the RCNT count, the sense voltage and resistance RSC of the selected memory cell 102 correspond to the complementary logic state, and the comparator 210 drives the data signal D high, indicating the selected memory cell stores the complementary logic state. (Column 4 lines 9-49)

As per claim 17, the examiner would like to point out that binning functions are well known in the art and it would have been an obvious design choice to bin a failed part.

Conclusion

This paper teaches a signal quality monitoring circuit that has a calculating circuit that reads the output of a counter provided for the output of a comparator. A memory records the counter output as a threshold value voltage. The calculation circuit determines the strong distribution of an electrical signal to measure the noise distribution of the electrical signal. A threshold value voltage generator supplies the

threshold value voltage, which changes at a fixed space, to the comparator. The comparator compares the multi-value electrical signal and the threshold value voltage, which changes at a fixed space.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cynthia Britt
Primary Examiner
Art Unit 2138